Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Canceled)

2-30. (Previously Canceled)

31. (New) A semiconductor memory device comprising:

a memory cell array in which a plurality of memory cells are arranged in a matrix, each storable n-valued data (n is a natural number equal to or larger than 2), each of the memory cells being configured by a nonvolatile memory; and

a write circuit which writes data into each of the memory cells and which, before storing next at least one-valued data into a first memory cell in which j-valued data ($j < n$) has been stored in the memory cell array, writes j or less-valued data into at least one of the memory cells adjacent to the first memory cell.

32. (New) The semiconductor memory device according to claim 31, wherein the memory cells constitute a NAND-type memory.

33. (New) The semiconductor memory device according to claim 31, wherein each of the memory cells is configured by an EEPROM.

34. (New) The semiconductor memory device according to claim 31, wherein the write circuit, when writing j or less-valued data into at least one of the adjacent memory cells, writes the data at a first threshold voltage lower than that

of the original data and, after having written the data into at least one of the adjacent memory cells, writes the data at a second threshold voltage higher than the first threshold voltage.

35. (New) The semiconductor memory device according to claim 34, wherein the write circuit writes j-valued data in the first memory cell at a second threshold voltage higher than the first threshold voltage simultaneously with the operation of writing next at least one-valued data in the first memory cell.

36. (New) The semiconductor memory device according to claim 31, wherein the memory cell array includes a second memory cell which acts as a flag and has at least a first and a second logic level.

37. (New) The semiconductor memory device according to claim 36, wherein the memory cell array, when reading the first memory cell, carries out a read operation suitable for the first threshold voltage in a case where the second memory cell is at the first logic level and carries out a read operation suitable for the second threshold voltage in a case where the second memory cell is at the second logic level.

38. (New) The semiconductor memory device according to claim 36, wherein the write operation, when writing j-valued data in the first memory cell at the second threshold voltage, writes data into the second memory cell and sets the second memory cell to one of the first and second logic levels.

39. (New) The semiconductor memory device according to claim 36, wherein the write circuit, when writing (j + 1)-valued data into the first memory cell, writes data into the second memory cell and changes the logic level of the second memory cell from the first logic level to the second logic level.

40. (New) The semiconductor memory device according to claim 37, wherein the write circuit, while writing j-valued data in the first memory cell at the second threshold voltage and writing (j + 1)-valued data in the first memory cell, writes data into the second memory cell and changes the logic level from the first logic level to the second logic level.

41. (New) The semiconductor memory device according to claim 37, wherein the memory cell array includes a plurality of second memory cells selected simultaneously with the first memory cell and, in a write operation, stores data of the same logic level into each of the second memory cells and, in a read operation, determines the first and second logic levels by a majority decision of the data read from said plurality of second memory cells.

42. (New) The semiconductor memory device according to claim 31, wherein the adjacent memory cells are the memory cells adjacent to the first memory cell along a word line.

43. (New) The semiconductor memory device according to claim 31, wherein the adjacent memory cells are the memory cells adjacent to the first memory cells along a bit line.

44. (New) A semiconductor memory device comprising:

a memory cell which stores k bits (k is a natural number equal to or larger than 2);

a plurality of storage circuits;

a first storage circuit of the storage circuits, which stores an input data;

a second storage circuit of the storage circuits, which stores the data read from the memory cell or the input data; and

a control circuit which, in a write operation, holds or changes the data in the first storage circuit or the data in the second storage circuit on the basis of the data stored in the memory cell and which, in the middle of a write operation, inputs next write data to the first storage circuit.

45. (New) The semiconductor memory device according to claim 44, wherein the first storage circuit is connected to a data line.

46. (New) The semiconductor memory device according to claim 44, wherein the second storage circuit is connected to the first storage circuit and the memory cell, the second storage circuit which outputs a signal indicating end of a verify operation.

47. (New) The semiconductor memory device according to claim 44, wherein the storage circuits include a third storage circuit which is connected to the memory cell, the first storage circuit and the second storage circuit, the third storage circuit which stores data from the memory cell.

48. (New) The semiconductor memory device according to claim 44, wherein the storage circuits include a fourth storage circuit which is connected between the second storage circuit and third storage circuit, the fourth storage circuit which stores data from the second storage circuit.

49. (New) The semiconductor memory device according to claim 44, wherein the memory cell is configured by an EEPROM.

50. (New) The semiconductor memory device according to claim 48, wherein the memory cell constitutes a NAND-type memory.

51. (New) A semiconductor memory device comprising:

a memory cell which has a threshold of k-value (k is a natural number equal to or larger than 2);

a first storage circuit which stores an input data from an outside;

a second storage circuit of the storage circuits, which stores data read from the memory cell or the input data; and

a control circuit which writes a threshold of n-value (n is a natural number equal to or smaller than k) into the memory cell according to the data of the

first and second storage circuits, and inputs next data from the outside to the first storage circuit when at least one value has written into the memory cell.

52. (New) A semiconductor memory device comprising:

a memory cell which has a threshold of k-value (k is a natural number equal to or larger than 2);

i storage circuits (i is a natural number equal to or larger than 2) store data read from the memory cell or data from an outside; and

a control circuit which writes a threshold of n-value (n is a natural number equal to or smaller than k) into the memory cell according to the data stored in the storage circuits, and inputs next data from the outside to at least one of the storage circuits when at least one value has written into the memory cell.